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METHOD AND SYSTEM FOR REDUCING THICKNESS OF SPIN-ON GLASS ON SEMICONDUCTOR WAFERS

TECHNICAL FIELD OF THE INVENTION

This invention relates generally to the field of semiconductor fabrication and, more specifically, to a method and system for reducing thickness of spin-on glass on semiconductor wafers.

BACKGROUND OF THE INVENTION

In semiconductor fabrication, one process that sometimes follows layering operations is a process called planarization. Planarization results in a smooth, planar surface for the semiconductor wafer and combats the effects of a varied wafer topography. Generally, as a semiconductor device is constructed using multiple surface layers and etchings, the surface of a semiconductor device becomes uneven. One planarization technique applies a layer of material to establish a smoother, flatter surface. One example of creating a planarization layer involves applying a liquid mixture of silicon dioxide in a solvent that evaporates quickly leaving a planarized film. Such a layer is called spin-on-glass ("SOG").

One drawback of using SOG is the added thickness that occurs near the outer edge of the semiconductor wafer. This added thickness frequently causes cracking when the SOG is hardened and/or densified. In addition, flaking occurs when a chemical mechanical polish is used on a wafer with SOG. The cracks and flakes can destroy integrated circuit dies built near the edge of the wafer thereby significantly reducing die yield. Advances in integrated circuit die fabrication have produced larger dies in recent years, thereby exacerbating this reduced die yield problem.

Few approaches have been attempted to solve the problems presented by the use of SOG. Some semiconductor manufacturers just live with these problems and scrap the defective dies. Others have tried to eliminate the problems by improving or altering the SOG process, such as changing the speed at which the liquid oxide is spun-on. But these approaches have not solved the problems. Another potential alternative is to use a solvent to dissolve the added thickness of the SOG. Semiconductor manufacturers use solvent to dissolve the outer two to three millimeters of the wafers so that the wafers can be handled by handling machinery. However, this dissolving process can not be extended to reduce the full width of the added thickness of the SOG near the outer edge because the process would disturb the SOG thickness needed at the wafer edge. An additional approach could be to use a dry etch process, but this would be very expensive and not cost-effective.

SUMMARY OF THE INVENTION

The challenges in the field of semiconductor fabrication continue to increase with demands for more and better techniques having greater flexibility and adaptability. Therefore, a need has arisen for a new method and system for reducing thickness of spin-on glass on semiconductor wafers.

In accordance with the present invention, a method and system for reducing thickness of spin-on glass on semiconductor wafers is provided that addresses disadvantages and problems associated with previously developed methods and systems.

According to one embodiment of the invention, a method for reducing thickness of spin-on glass on semiconductor wafers includes rotatably mounting a semiconductor wafer and positioning a grinding member proximate an outer edge of the semiconductor wafer. The method further includes rotating both the semiconductor wafer and the grinding member, and engaging the rotating grinding member with the outer edge of the rotating semiconductor wafer while applying a chemical to the outer edge.

According to another embodiment of the invention, a method for reducing thickness of spin-on glass on semiconductor wafers includes rotatably mounting a semiconductor wafer and positioning a grinding member proximate an outer edge of the semiconductor wafer. The method further includes rotating both the semiconductor wafer and the grinding member, and engaging the rotating grinding member with the outer edge of the rotating semiconductor wafer while applying deionized water to approximately the center of the rotating semiconductor wafer.

According to an additional embodiment of the invention, a method for reducing thickness of spin-on glass on semiconductor wafers includes providing a chemical in a container, rotatably mounting a semiconductor wafer, and bearing a grinding member against a portion of an outer edge of the semiconductor wafer. The method further includes rotating the semiconductor wafer while the semiconductor wafer is in contact with the grinding member and while the portion of the outer edge of the semiconductor wafer is immersed in the chemical.

Embodiments of the invention provide numerous technical advantages. For example, integrated circuit die yield is improved according to one embodiment of the present invention. According to that embodiment, useable dies may be fabricated on locations at the wafer within approximately 3 mm of the semiconductor wafer edge, thereby resulting in significant savings and cost-effectiveness. Other technical advantages are readily apparent to one skilled in the art from the following figures, descriptions, and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the invention, and for further features and advantages, reference is now made to the following description, taken in conjunction with the accompanying drawings, in which:

FIGURE 1 is a cross-sectional view of a semiconductor wafer having various layers including a spin-on glass ("SOG") layer with a SOG protuberance;

FIGURE 2A is a schematic diagram illustrating one method of reducing thickness of spin-on glass on semiconductor wafers in accordance with one embodiment of the present invention;

FIGURE 2B is a flowchart generally outlining the method shown in FIGURE 2A;

FIGURE 3A is a schematic diagram illustrating another method of reducing thickness of SOG on semiconductor wafers in accordance with one embodiment of the present invention;

FIGURE 3B is a flowchart generally outlining the method shown in FIGURE 3A;

FIGURE 4A is a schematic diagram illustrating an additional method of reducing thickness of SOG on semiconductor wafers in accordance with one embodiment of the present invention; and

FIGURE 4B is a flowchart generally outlining the method shown in FIGURE 4A.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

Embodiments of the present invention and their advantages are best understood by referring now to FIGURES 1 through 4B of the drawings, in which like numerals refer to like parts.

FIGURE 1 is a cross-sectional view of one embodiment of a semiconductor wafer 100 having a substrate 102, a spin-on glass ("SOG") layer 104 disposed outwardly from substrate 102, and a SOG protuberance 106 disposed outwardly from, and near a side edge 118 of, substrate 102. Semiconductor wafer 100 is used in the fabrication of integrated circuit dies for use in, for example, electronic and telecommunications devices. Therefore, semiconductor wafer 100 may have many different types of layers or regions, such as a transistor circuitry region 108, a metal oxide layer 110, and a metallization region 112 as shown in FIGURE 1. The number and type of layers and regions depends on the type of integrated circuit fabricated on substrate 102.

Substrate 102 can be any suitable material used in semiconductor fabrication, such as a silicon wafer or a germanium wafer. SOG layer 104 is a planarization layer well known in the art of semiconductor fabrication. The application of SOG layer 104 to semiconductor wafer 100 is one of many planarization techniques used in semiconductor wafer fabrication. In one embodiment, the application of SOG layer 104 involves applying a liquid mixture of silicon dioxide, or other silicate, in a solvent while the associated wafer is spun. The solvent evaporates quickly leaving a planarized film. One drawback of using SOG layer 104 is that SOG protuberance 106 forms on outer edge 116 of semiconductor wafer 100 due to the centrifugal force acting on the liquid mixture as a result of the spinning of semiconductor wafer 100.

SOG protuberance 106 frequently causes cracks 114 when the SOG is hardened and/or densified, or if a solvent is used to dissolve a portion of outer edge 116 for handling purposes. In addition, flaking can occur if a chemical mechanical polish ("CMP") is used on semiconductor wafer 100. Cracks 114 and flakes can destroy integrated circuit dies that are built in close proximity to side edge 118 of semiconductor wafer 100, thereby significantly hurting die yield.

SOG protuberance 106 forms on an outer edge 116 on semiconductor wafer 100, and is usually no more than approximately ten millimeters from side edge 118, as illustrated. Semiconductor manufacturers strive to build integrated circuit dies as close to side edge 118 as possible to maximize the number of dies produced on each wafer. Currently, the only restraint on the proximity of dies to side edge 118 are those imposed by wafer handling equipment. As a result, manufacturers desire to build integrated circuit dies up to approximately three millimeters from side edge 118. The present invention addresses reducing the thickness of SOG protuberance 106 on semiconductor wafer 100. One such method is illustrated in FIGURES 2A and 2B.

FIGURES 2A and 2B illustrate one method of reducing the thickness of SOG protuberance 106 on semiconductor wafer 100 in accordance with the present invention. A chemical 212 is provided in a container 210 at step 200. In one embodiment, chemical 212 is a hydrofluoric acid; however, chemical 212 may be other types of chemicals suitable for etching SOG protuberance 106, such as an aluminum oxide or silicon dioxide. Container 210 may be any type or size of container suitable to hold chemical 212.

Semiconductor wafer 100 is rotatably mounted at step 202. In one embodiment, semiconductor wafer 100 is secured in a substantially vertical position; however, semiconductor wafer 100 may be secured in other suitable positions. In one embodiment, semiconductor wafer 100 is secured to a spindle 214 with a vacuum chuck, which is well known in the art of semiconductor fabrication; however, semiconductor wafer 100 may be secured to spindle 214 using other suitable methods.

A grinding member 218 is disposed against a portion 216 of an outer edge 220 of semiconductor wafer 100, at step 204. Outer edge 220 typically corresponds to a portion of semiconductor wafer 100 having SOG protuberance 106. In one embodiment, grinding member 218 is a scrubber mechanism used in the CMP process; however, grinding member 218 may be other types of members with abrasive materials for abrading SOG protuberance 106. Grinding member 218 is mounted in any suitable manner. For example, grinding member 218 may be spring-loaded so that a substantially constant force is applied to SOG protuberance 106, or grinding member 218 may be pneumatically, hydraulically, or electrically controlled so that

grinding member 218 reduces a predetermined amount of SOG thickness per unit time. Grinding member 218 may also be angled as desired, such that the depth of grinding is controlled by stopping grinding member 118 when it reaches substrate 102.

At step 206, semiconductor wafer 100 is rotated while semiconductor wafer 100 is in contact with grinding member 118 and while portion 216 of outer edge 220 is immersed in chemical 212. As a result, grinding member 218, in conjunction with chemical 212, reduces the thickness of SOG protuberance 106 to a desired level. SOG layer 104 may then be densified knowing that cracking and flaking will be significantly reduced. This allows die yield to be improved, thereby significantly enhancing cost-effectiveness.

FIGURES 3A and 3B illustrate another method of reducing the thickness of SOG protuberance 106 on semiconductor wafer 100 in accordance with the present invention. Semiconductor wafer 100 is rotatably mounted at step 300. In one embodiment, semiconductor wafer 100 is secured in a substantially horizontal position; however, semiconductor wafer 100 may be secured in other suitable positions, such as a substantially vertical position. In one embodiment, semiconductor wafer 100 is secured to a spindle 320 with a vacuum chuck, which is well known in the art of semiconductor fabrication; however, semiconductor wafer 100 may be secured to spindle 320 using other suitable methods.

A grinding member 322 is positioned proximate an outer edge 328 of semiconductor wafer 100, at step 302. In one embodiment, grinding member 322 is an ultra-fine grit grinding wheel; however, grinding member 322 may be other types of rotatable mechanisms with abrasive materials used for reducing the thickness of SOG protuberance 106. Grinding member 322 is mounted in any suitable manner. As described above with grinding member 218, grinding member 322 may be spring-loaded so that a substantially constant force is applied to SOG protuberance 106, or grinding member 322 may be pneumatically, hydraulically or electrically controlled so that grinding member 322 reduces a predetermined amount of SOG thickness per unit time. Alternatively, grinding member 322 may be manually controlled.

Semiconductor wafer 100 is rotated, at step 304, and grinding member 322 is rotated, at step 306. Both semiconductor wafer 100 and grinding member 322 may be rotated in either a clockwise or counterclockwise direction. A chemical 324 is applied to outer edge 328 of semiconductor wafer 100, at step 308. In one embodiment, chemical 324 is a hydrofluoric acid; however, chemical 212 may be other types of chemicals suitable for etching SOG protuberance 106, such as an aluminum oxide or silicon dioxide. In one embodiment, chemical 324 is applied to outer edge 328 with a syringe 326; however, chemical 324 may be applied to outer edge 328 using other suitable methods that allow localized application.

Rotating grinding member 322 is engaged with outer edge 328 of rotating semiconductor wafer 100, at step 310, such that grinding member 322, in conjunction with chemical 324, reduces the thickness of SOG protuberance 106 to a desired level. Rotating grinding member 322 is then disengaged so that rotating semiconductor wafer 100 may be rinsed, at step 312. SOG layer 104 may then be densified knowing that cracking and flaking will be significantly reduced. This allows die yield to be improved, thereby significantly enhancing cost-effectiveness.

FIGURES 4A and 4B illustrate another method of reducing the thickness of SOG protuberance 106 on semiconductor wafer 100 in accordance with the present invention. Semiconductor wafer 100 is rotatably mounted at step 400. In one embodiment, semiconductor wafer 100 is secured in a substantially horizontal position; however, semiconductor wafer 100 may be secured in other suitable positions, such as a substantially vertical position. In one embodiment, semiconductor wafer 100 is secured to a spindle 420 with a vacuum chuck, which is well known in the art of semiconductor fabrication; however, semiconductor wafer 100 may be secured to spindle 420 using other suitable methods.

A grinding member 422 is positioned proximate an outer edge 428 of semiconductor wafer 100, at step 402. In one embodiment, grinding member 422 is an ultra-fine grit grinding wheel; however, grinding member 422 may be other types of rotatable mechanisms with abrasive materials used for reducing the thickness of SOG protuberance 106. Grinding member 422 is mounted in any suitable manner. As described above in conjunction with grinding members 218 and 322, grinding

member 422 may be spring-loaded so that a substantially constant force is applied to SOG protuberance 106, or grinding member 422 may be pneumatically, hydraulically or electrically controlled so that grinding member 422 reduces a predetermined amount of SOG thickness per unit time. Alternatively, grinding member 422 may be manually controlled.

Semiconductor wafer 100 is rotated, at step 404, and grinding member 322 is rotated, at step 406. Both semiconductor wafer 100 and grinding member 422 may be rotated in either a clockwise or counterclockwise direction. A deionized water 424 is applied to approximately the center of rotating semiconductor wafer 100, at step 408. Deionized water 424 is used to rinse semiconductor wafer 100, thereby facilitating particle and chemical removal. The present invention contemplates the use of other deionized liquids to rinse semiconductor wafer 100. In one embodiment, deionized water 424 is applied to approximately the center of rotating semiconductor wafer 100 with a syringe 426; however, deionized water 424 can be applied to approximately the center of rotating semiconductor wafer 100 using other suitable methods that allow localized application.

Rotating grinding member 422 is engaged with outer edge 428 of rotating semiconductor wafer 100, at step 410, such that grinding member 422 reduces the thickness of SOG protuberance 106 to a desired level. Rotating grinding member 322 is then disengaged, at step 412, so that rotating semiconductor wafer 100 may be rinsed. SOG layer 104 may then be densified knowing that cracking and flaking will be significantly reduced. This allows die yield to be improved, thereby significantly enhancing cost-effectiveness.

Although embodiments of the invention and their advantages are described in detail, a person skilled in the art could make various alternations, additions, and omissions without departing from the spirit and scope of the present invention as defined by the appended claims.